Listing of Claims:

1. (Currently Amended) A resistor having a resistance that can be adjusted by current being passed there through and which is formed as part of a semiconductor device comprising:

a polycrystalline silicon resistor formed of and on a layer, wherein said polysilicon resistor is formed using a doping wherein said doping has a concentration of from ~$6x10^{19}$ cm^{-3} to ~[3.75] $1x10^{20}$ cm^{-3} and wherein said polycrystalline silicon resistor has at least a first and second order temperature coefficient, wherein the sign of said first and second order temperature coefficients are opposite each other; and

wherein said resistor resistance is electronically [trimmed] trimmable within a range from 60% to 30 % of original value and

further wherein said doping produces a fine grain size and an increased grain boundary density .

2. (Currently Amended) A resistor having a resistance that can be adjusted by current being passed there through and which is formed as part of a semiconductor device comprising:

a polycrystalline silicon resistor formed of on a layer, wherein said polysilicon resistor is formed using a doping wherein said doping has a concentration of less than ~$3.75x10^{20}$ cm^{-3} and wherein said polycrystalline silicon resistor has at least a first and second order temperature coefficient, wherein the sign of said first and second order temperature coefficients are opposite each other; and

wherein said resistor resistance is electronically trimmed [trimmed] trimmable within a range from 60% to 30 % of original value and

further wherein said doping produces a fine grain size and an increased grain boundary density..

3. (Cancelled) A method of making a polysilicon resistor comprising the steps of:

providing a substrate,

depositing a polycrystalline layer on said substrate,

aligning and exposing a poly resistor mask,

poly doping the polycrystalline layer,

forming an insulating oxide,

aligning and exposing the mask for the resistor,

depositing an inter level dielectric,

annealing the inter level dielectric, and

completing the processing using low temperature processing.

4. (Cancelled) A method as in Claim 3 wherein said first annealing step occurs at or below 900 °C.

5. (Cancelled) A method as in Claim 3 wherein said formation of said insulating oxide occurs at or below 950 °C .

6.(Cancelled) A method as in Claim 3 wherein said ion implantation to provide the poly doping results in a concentration of ~$6x10^{19}$ cm^{-3} to ~$3.75x10^{20}$ cm^{-3} .

7. (Cancelled) A method of trimming a polysilicon resistor to a target resistance formed using a low concentration doping comprising the steps of:

passing an electrical signal through said resistor,

measuring and increasing said passed electrical signal until the resistance of said resistor equals the target resistance.

Cont D1

8. (Cancelled) A method of trimming a polysilicon resistor to a target resistance formed using a low concentration doping, as in claim 7 wherein the step of passing am electrical signal is by way of a current pulse through said resistor and said method further comprises:

measuring and increasing said passed current pulse until the resistance of said resistor equals the target resistance.

9. (Cancelled) A method of trimming a polysilicon resistor to a target resistance formed using a low concentration doping as in claim 7 wherein the step of passing a current pulse through said resistor is less than 20mA.

10.(Cancelled) A method of trimming a polysilicon resistor to a target resistance formed using a low concentration doping as in claim 7 wherein the step of passing a current pulse through said resistor is done a voltage less than 16V.

11. (Currently Amended) A resistor having a resistance that can be adjusted by current being passed there through and which is formed as part of a semiconductor device comprising:

a polycrystalline silicon resistor formed of on a layer, wherein said polysilicon resistor is formed using a dopng wherein said doping has a concentration of greater than ~$6x10^{19}$ cm^{-3} and wherein said polycrystalline silicon resistor has at least a first and second order temperature coefficient, wherein the sign of said first and second order temperature coefficients are opposite each other; and

wherein said resistor resistance is electronically trimmed [trimmed] trimmable and further wherein said doping produces a fine grain size and an increased grain boundary density .

12. (Currently Amended) A resistor having a resistance that can be adjusted by current being passed there through and which is formed as part of a semiconductor device comprising:

a polycrystalline silicon resistor formed of on a layer, wherein said polysilicon resistor is formed using a late implant doping technique and wherein said polycrystalline silicon resistor has at least a first and second order temperature coefficient, wherein the sign of said first and second order temperature coefficients are opposite each other; and

wherein said resistor resistance is electronically trimmed [trimmed] trimmable and further wherein said doping produces a fine grain size and an increased grain boundary density.

13. (Cancelled) A method as in Claim 3 wherein said final annealing step occurs at or below 900 °C .

14. (Cancelled) A method of trimming a polysilicon resistor to a target resistance formed using a low concentration doping as in claim 7 wherein the electrical signal that is passed is less than 16V.

15. (Cancelled) A method as in claim 3 further comprising the step of forming a field oxide layer prior to the depositing of said polycrystaline layer.